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Serial No.:

09/494,567

Applicant(s):

Vorbach et al.

Filing Date:

Group Art Unit:

2661

U. S. PATENT DOCUMENTS							
EXAMINER'S	PATENT/	PATENT/	NAME	CLASS	SUB	FILING]
. INITIALS	PUBLICATION	PUBLICATION		İ	CLASS	DATE*	
	NUMBER	DATE					
TM	2,067,477	January 12, 1937	J.B. Cooper	\		/	1
TM	3,242,998	March 29, 1966	C.H. Gubbins			7	1
TM	3,681,578	August 1, 1972	Stevens				1
TM	3,757,608	September 11, 1973	Willner				
TM	3,855,577	December 17, 1974	Vandierendonck			7	1
TM	4,498,172	February 5, 1985	Bhavsar				
TM	4,566,102	January 21, 1986	Hefner	1		7	
TM	4,663,706	May 5, 1987	James et al.				
· TM	4,682,284	July 21, 1987	Schrofer				1
TM	4,720,780	January 19, 1988	Dolecek				1
· M	4,852,043	July 25, 1989	Guest				1
TM	4,860,201	August 22, 1989	Miranker et al.		X		1
TM	4,891,810	January 2, 1990	de Corlieu et al.				1
TM	4,910,665	March 20, 1990	Mattheyses et al.				1
TM	5,047,924	September 10, 1991	Matsubara et al.		/	-	1
TM	5,065,308	November 12, 1999	Evans		/		1
-TM	5,072,178	December 10, 1991	Matsumoto				1
TM	5,144,166	September 1, 1992	Camarota et al.				1
TM	5,193,202	March 9, 1993	Lee et al.				1
TM	5,203,005	April 13, 1993	Horst				1
TM	5,274,593	December 28, 1993	Proebsting				
TM	5,294,119	March 15, 1994	Vincent et al.	/]
	5,301,284	April 5, 1994	Estes et al.	CONSID	ERED ON	7/11/05	TM
• .	5,347,639	September 13, 1994	Rechtschaffen et al.	CONSIC		7/11/05	1 /
TM	5,349,193	September 20, 1994	Mott et al.				''''
TM	5,353,432	October 4, 1994	Richek et al.				
TM	5,379,444	January 3, 1995	Mumme				1
	5,410,723	April 25, 1995	Schmidt et al.	CONSI	DERED ON	17/11/05	TM
·TM	5,425,036	June 13, 1995	Liu et al.			71118	
TM	5,428,526	June 27, 1995	Flood et al.				
	5,465,375	November 7, 1995	Thepaut et al.	CONSIDE	RED ON	7/11/05	TM
```	5,475,856	December 12, 1995	Kogge	CONSIDE		7/11/05	m
TM	5,530,873	June 25, 1996	Takano			//	<b>'</b> '' `
TM	5,530,946	June 25, 1996	Bouvier et al.				1
M	5,574,930	November 12, 1996	Halverson Jr. et al.				
	5,600,265	February 4, 1997	El Gamal Abbas et		X		
TM			al.				1
TM	5,611,049	March 11, 1997	Pitts				
TM	5,625,806	April 29, 1997	Kromer				

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1/8 January 17,2006

EXAMINER'S ' INITIAL\$	PATENT/ ,PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLASS	SUB CLASS	FILING DATE
	5,649,176	July 15, 1997	Selvidge et al.		1,82	
	5,649,179	July 15, 1997	Steenstra et al.			
	5,655,069	August 5, 1997	Ogawara et al.		(1)	<del></del>
	5,657,330	August 12, 1997	Matsumoto		7 10	
	5,675,743	October 7, 1997	Mavity	C	100	· · · · · · · · · · · · · · · · · · ·
	5,680,583	October 21, 1997	Kuijsten	7	1,11	
	5,717,943	February 10, 1998	Barker et al.	10	7/,	
	5,732,209	March 24, 1998	Vigil et al.	7	0	
	5,754,827	May 19, 1998	Barbier et al.	14		<del></del>
	5,760,602	June 2, 1998	Tan			
	5,773,994	June 30, 1998	Jones			
	5,784,636	July 21, 1998	Rupp			
	5,794,059	August 11, 1998	Barker et al.			
	5,794,062	August 11, 1998	Baxter			
	5,802,290	September 1, 1998	Casselman			
	5,828,229	October 27, 1998	Cliff et al.			
·	5,848,238	December 8, 1998	Shimomura et al.			
	5,854,918	December 29, 1998	Baxter		•	
	5,859,544	January 12, 1999	Norman			
	5,865,239	February 2, 1999	Carr			
	5,867,723	February 2, 1999	Peters et al.			
	5,884,075	March 16, 1999	Hester-et al.			
	5,887,162	March 23/1999	Williams et al.			,
	5,889,982	March 30, 1999	Rodgers et al.			
	5,892,370	April 6, 1999	Eaton et al.			
	5,901,279	May 4, 1999	Davis III			
	5,924,119	July 13, 1999	Sindhu et al.			
	5,933,642	August 3, 1999	Baxter et al.			
	5,966,534	October 12, 1999	Cooke et al.			
	5,970,254	October 19, 1999	Cooke et al.			
	6,011,407	January 4, 2000	New			
	6,021,490	February 1, 2000	Vorbach et al.			
	6,023,564	February 8, 2000	Trimberger			
	6,023,742	February 8, 2000	Ebeling et al.			
•	6,034,538	March 7, 2000	Abramovici			
	ø,038,650	March 14, 2000	Vorbach et al.			
	6,038,656	March 14, 2000	Cummings et al.			
	6,047,115	April 4, 2000	Mohan et al.			
	6,049,222	April 11, 2000	Lawman			
	6,058,469	May 2, 2000	Baxter			
	6,081,903	June 27, 2000	Vorbach et al.	-1		
	6,085,317	July 4, 2000	Smith		-	
	6,086,628	July 11, 2000	Dave et al.			
	6,088,795	July 11, 2000	Vorbach et al.			

EXAMINER'S · INITIALS	PATENT/ ,PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLASS	SUB CLASS	FILING DATE
	6,092,174	July 18, 2000	Roussakov			
	6,105,105	August 15, 2000	Trimberger et al.			0/
	6,119,181	September 12, 2000	Vorbach et al.	<del></del>		D/ \\
	6,125,408	September 26, 2000	McGee et al.		100	111
	6,172,520	January 9, 2001	Lawman et al.			0,1:
	6,173,434	January 9, 2001	Wirthlin et al.	<u> </u>	194	
	6,202,182	March 13, 2001	Abramovici et al.		40×10	
	6,219,833	April 17, 2001	Solomon et al.	/	7	-
	6,230,307	May 8, 2001	Davis et al.			
	6,243,808	June 5, 2001	Wang	W		
	6,260,179	July 10, 2001	Ohsawa et al.	7		
	6,263,430	July 17, 2001	Trimberger et al.			· · · · · · · · · · · · · · · · · · ·
	6,279,077	August 21, 2001	Nasserbakht et al.			-
	6,282,627	August 28, 2001	Wong et al.			
	6,288,566	September 11, 2001	Hanrahan et al.			
	6,289,440	September 11, 2001	Casselman			
	6,298,472	October 2, 2001	Phillips et al.			
	6,311,200	October 30, 2001	Hanrahan et al.			
	6,321,366	November 20, 2001	Tseng et al.			
	6,321,373	November 20, 2001	Ekanadham et al.			
	6,338,106	January 8, 2002	Vorbach et al.			
	6,341,318	January 22, 2002	Dakhil			
	6,347,346	February 12, 2002	Taylor			
	6,349,346	February 19, 2002	Hanrahan et al.			
	6,370,596	April 9, 2002	Dakhil			
	6,378,068	April 23, 2002	Foster et al.			
	6,389,379 6,389,579	May 14, 2002 May 14, 2002	Lin et al.			
	6,392,912	May 21, 2002	Phillips et al.  Hanrahan et al.		<del></del>	
	6,405,299	June 11, 2002	Vorbach et al.			
	6,421,817/	July 16, 2002	Mohan et al.			
	6,425,068	July 23, 2002	Vorbach et al.			
	6,457,116	September 24, 2002	Mirsky et al.			
	6,A77,643	November 5, 2002	Vorbach et al.			<del></del>
	6,480,937	November 12, 2002	Vorbach et al.			
	6,480,954	November 12, 2002	Trimberger et al.			
-	6,513,077	January 28, 2003	Vorbach et al.			
-	6,519,674	February 11, 2003	Lam et al.			
/	6,526,520	February 25, 2003	Vorbach et al.			
	6,538,468	March 25, 2003	Moore			
	6,539,477	March 25, 2003	Seawright			
	6,542,998	April 1, 2003	Vorbach et al.			
	6,571,381	May 27, 2003	Vorbach et al.			
	6,587,939	July 1, 2003	Takano			
/						

EXAMINER'S	PATENT/	PATENT/	NAME	CLASS	SUB	FILING
INITIALS	PUBLICATION	<b>PUBLICATION</b>			CLASS	DATE*
	NUMBER	DATE			(02.200	
	6,657,457	December 2, 2003	Hanrahan et al.		16	/
	6,697,979	February 24, 2003	Vorbach et al.			
	6,687,788	February 3, 2004	Vorbach et al.		(4)	
	2002/0038414	March 28, 2002	Taylor et al.	`	01/10	
	2002/0143505	October 3, 2002	Drusinsky	(	$\frac{1}{2}$	
	2002/0144229	October 3, 2002	Hanrahan	/	/\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
	2002/0165886	November 7, 2002	Lam	7	0,	
	2003/0123579	July 3, 2003	Safavi et al.	17		
	2003/0014743	January 16, 2003	Cooke et al.	1/1/	<del>_</del>	
	2003/0046607	March 6, 2003	Vorbach			
	2003/0052711	March 20, 2003	Taylor et al.			
	2003/0055861	March 20, 2003	Lai et al.			
	2003/0056085	March 2, 2003	Vorbach		-	
	2003/0056091	March 20, 2003	Greenberg			
	2003/0056202	March 20, 2003	Yorbach		-	
	2003/0093662	May 15, 2003	Vorbach et al.			
	2003/0097513	May 22, 2003	Yorbach et al.			
	2003/0135686	July 17, 2003	Vorbach et al.			
	2004/0015899	January 22, 2004	May et al.			
	2004/0025005	February 5, 2004	Vorbach et al.			· · · · · · · · · · · · · · · · · · ·

FOREIGN PATENT DOCUMENTS

EXAMINER'S	DOCUMENT	DATE	COUNTRY	CLASS	SUB-CLASS	TRANS	LATION
INITIALS	NUMBER					YES	NO
	0 463 721	January 2, 1992	Europe		<u> </u>		-
	0 477 809	April 1, 1992	Europe				<del>                                     </del>
	0 485 690	May 20, 1992	Europe				
	0 497 029	August 5, 1992	Europe				<del>                                     </del>
	0 628 917	December 14, 1994	Europe				
	0 686 915	December 13, 1995	Europe				
	0 726 532	July 2, 1998	Europe	···			<u> </u>
	0 835 685	October 2, 1996	Europe				<u> </u>
	0 926 594	June 30, 1999	Europe				<u> </u>
	1 102 674	July 13, 1999	Europe				
	1 146 432	October 17, 2001	Europe				
	42 21 278	January 5, 1994	Germany				
•	38 55 673	November 20, 1996	Germany				
	100 28/397	December 20, 2001	Germany				
	100 36 627	February 14, 2002	Germany				
	10/1 29 237	April 18, 2002	Germany				
	102 04 044	August 14, 2003	Germany	····			
/	196 54 593	July 2, 1998	Germany				<del>                                     </del>
	197 04 044	August 13, 1998	Germany				
	197 04 742	September 24, 1998	Germany				

<u> </u>	198 07 872	August 26, 1999	Germany			/	Τ
	198 61 088	February 10, 2000	Germany	<u> </u>		/	
	199 26 538	December 14, 2000	Germany			/	<del>                                     </del>
	WO98/26356	June 18, 1998	PCT			/	<del>                                     </del>
	WO98/28697	July 2, 1998	PCT				<del>                                     </del>
	WO98/29952	July 9, 1998	PCT		0/		
	WO98/31102	July 16, 1998	PCT		(A)		<del> </del>
	WO98/35299	August 13, 1998	PCT				<del> </del>
	WO99/00731	January 7, 1999	PCT		10		
	WO99/00739	January 7, 1999	PCT		\$7		
	WO99/32975	July 1, 1999	PCT				
	WO99/40522	August 12, 1999	PCT		0,1		
	WO99/44147	September 2, 1999	PCT	, /			
	WO99/44120	September 2, 1999	PCT	1	\		
	WO00/17771	March 30, 2000	PCT	17 1	1		
	WO00/38087	June 29, 2000	PCT	A		-	
	WO00/77652	December 21, 2000	PCT	/			
•	WO02/13000	February 14, 2002	PCT				
	WO02/21010	March 14, 2002	PCT				
	WO02/29600	April 11, 2002	РСТ				
	WO02/71248	September 12, 2002	PCT				
	WO02/71249	September 12, 2002	PCT				
	WO02/103532	December 27, 2002	PCT				
	WO03/17095	February 27, 2003	PCT			<del> </del>	
	WO03/23616	March 30, 2003	PCT				
	WO03/25781	March 27, 2003	PCT				
	WO03/32975	April 24, 2003	PCT				
	WO03/36507	May 1, 2003	PCT		<del></del>		

## OTHER DOCUMENTS

EXAMINER'S	AUTHOR TITLE DATE DEPTRIENT BACES FTC
INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Arabi et al., "PLD Integrates Dedicated High-speed Data Buffering, Complex State Machine, and Fast Decode Array," conference record on WESCON '93, Sep. 28, 1993, pp. 432-436
	Ade et al., "Minimum Memory Buffers in DSP Applications," Electronics Letters, vol. 30, No. 6, March 17, 1994, pp. 469-471
	Villasenor, John et al., "Configurable Computing," Scientific American, Vol. 276, No. 6, June 1997, pp. 66-71.
•	Villasenor, John et al. "Configurable Computing Solutions for Automatic Target Recognition," IEEE, 1996 pp. 70-79.
-	Tau, Edward et al. "A First Generation DPGA Implementation," FPD'95, pp. 138-143
	Athanas, Peter et al., "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines," IEEE Symposium on FPGAs For Custom Computing Machines, IEEE Computer Society Press, April 19-21, 1995, pp. i-vii, 1-222
	Athanas, Peter et al., "An Adaptive Hardware Machine Architecture and Compiler for Dynamic Processor Reconfiguration", IEEE, Laboratory for Engineering Man/Machine Systems Division of Engineering, Box D, Brown University Providence, Rhode Island, 1991, pages 397-400
	Bittney, Ray A. Jr., "Wormhole Run-time Reconfiguration: Conceptualization and VLSI Design of a High Performance Computing System," Dissertation, January 23, 1997, pp. I-XX, 1-415
	Myers, G. "Advances in Computer Architecture," Wiley-Interscience Publication, 2nd ed., John Wiley &

LAAVINER'S NITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Sons, Inc. pp. 463-94, 1978.
	M. Saleeba, "A Self-Contained Dynamically Reconfigurable Processor Architecture," Sixteenth Australian
	Computer Science Conference, ASCS-16, QLD, Australia, February, 1993.
	M. Morris Mano, "Digital Design," by Prentice Hall, Inc., Englewood Cliffs, New Jersey 07682, 1984, pp. 119-125, 154-161.
	Maxfield, C. "Logic that Mutates While-U-Wait" EDN (Bur. Ed) (USA), EDN (European Edition), 7 November 1996, Cahners Publishing, USA
	Norman, Richard S., "Hyperchip Business Summary, The Opportunity," January 31, 2000, pages 1-3.
	Ferrante J. et al., "The Program Dependence Graph and its Use in Optimization ACM Transactions on Programming Languages and Systems," July 1987, USA, [online] Bd. 9, Nr. 3, pages 319-349, XP002156651 ISSN: 0164-0935 ACM Digital Library
	Hwang L. et al., "Min-cut Replication in Partitioned Networks" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, [online] Bd. 14, Nr. 1, Ianuary 1995, pages 96-106, XP00053228 USA ISSN: 0278-0070 IEEE Xplore
	Baumgarte, V., et al., PACT XPP "A Self-reconfigurable Data Processing Architecture," PACT Info. GMBH, Munchen Germany 2001
	Jantsch, Axel et al., "A Case Study on Hardware/software Partitioning," Royal Institute of Technology, Kista, Sweden, April 10, 1994 IEEE, pp. 111-118
	Becker, J. et al., "Parallelization in Co-compilation for Configurable Accelerators - a Host/accelerator Partitioning Compilation Method," proceedings of Asia and South Pacific Design Automation Conference, Yokohama, Japan, February 10-13, 1998
	Isshiki, Tsuyoshi et al., "Bit-Serial Pipeline Synthesis for Multi-FPGA Systems with C++ Design Capture," 1996 IEEE, pp. 38-47
	Weinhardt, Markus, "Ubersetzingsmethoden für strukturprogrammierbare rechner," Dissertation for Doktors der Ingenieurwissenschaften der Universitat Karlstyche: July 1, 1997 [Weinhardt, M. "Compilation Methods for Structure-programmable Computers", dissertation, ISBN 3-89722-011-3, 1997]
	Hammes, Jeff et al., "Cameron: High Level Language Compilation for Reconfigurable Systems," Department of Computer Science, Colorado State University, Conference on Parallel Architectures and Compilation Techniques, October 12-16, 1999
	K. Wada et al., "A Performance Evaluation of Tree-based Coherent Distributed Shared Memory" Proceedings of the Pacific RIM Conference on Communications, Comput and Signal Processing, Victoria, May 19-21 1993
	Nilsson et al., "The Scalable Tree Protocol - A Cache Coherence Approaches for Large-Scale Multiprocessors" IEEE, pp. 498-506 December 1992
	Wu et al., "A New Cache Directory Scheme", IEEE, pp 466-472, June 1996
	Hauck "The Roles of FPGA's in Reprogrammable Systems," IEEE, April 1998, pp. 615-638
	Wittig et al., "OneChip: An FFGA Processor with Reconfigurable Logic" IEEE, 1996 pp. 126-135
	Cadambi et al., "Managing Pipeline-reconfigurable FPGAs," ACM, 1998, pp. 55-64
	Hong Yu Xu et al., "Parallel QR Factorization on a Block Data Flow Architecture" Conference Proceeding Article, March 1, 1992, pages 332-336 XPO10255276, PAGE 333, Abstract 2.2, 2.3, 2.4 - page 334
	Mirsky, E. DeHon, "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, 1996, PP. 157-1666
	Cardoso, J.M.P. Compilation of Java TM Algorithms onto Reconfigurable Computing Systems with Exploitation of Operation-Level Parallelism, Ph.D. Thesis, Universidade Tecnica de Lisboa (UTL), Lisbon, Portugal October 2000 (English Abstract included)
	Kung, "Dezdlock Avoidance for Systolic Communication", 1988 Conference Proceedings of 15th Annual International Symposium on Computer Architecture, May 30, 1988, pp. 252-260
	TMS320C54X DSP: CPU and Peripherals, Texas Instruments, 1996, pp. 6-26 to 6-46
	TMS320C54x DSP: Mnemonic Instruction Set, Texas Instruments, 1996, p. 4-64
	XLINX, "Logic Cell Array Families: XC4000, XC4000A and XC4000H", product description, pages 2-7 to 2/15, Additional XC3000, XC31000 and XC3100A Data, pages 8-16 and 9-14

	AVERTION STEELS AND ADDRESS AN						
- INITIALS	AUTHOR, TITLE, DATE, PERTINENT PA						
	Miller, Michael J. et al., "High-Speed FIFOs Contend with Widely Diff Buffer and Dual-pointer System Provide Rapid, High-density Data Stor Design, September 1, 1985, pages 83-86.	rage and Reduce Overhead", Compute					
	Forstner, Peter "Wer Zuerst Kommt, Mahlt Zuerst!: Teil 3: Einsatzgebi FIFO-Speichern", Elektronik, August 2000, pages 104-109						
	John R. Hauser et al., "Garp: A MIPS Processor with a Reconfigurable California, Berkeley, IEEE, 1997, pages 12-21	Coprocessor", University of					
	Jorg Donandt, "Improving Response Time of Programmable Logic Controllers by Use of a Boolean Coprocessor", AEG Research Institute Berlin, IEEE, 1989, pages 4-167 - 4-169.						
	Alexandre F. Tenca et al., "A Variable Long-Precision Arithmetic Unit Coprocessor Architectures", University of California, Los Angeles, 199	Design for Reconfigurable 8, pages 216 - 223					
	Andreas Koch et al, "Practical Experiences with the SPARXIL Co-Proc	essor 1998, IEEE, pages 394 - 398					
	Gokhale M. B. et al., "Automatic Allocation of Arrays to Memories in Memory Banks", Field-Programmable Custom Computing Machines,	999) VEEB pages 63-67					
	Christian Siemers, "Rechenfabrik Ansaetze Fuer Extrem Parallele Proze Hannover, DE No. 15, July 16, 2001, pages 170-179	essoren" (Verlag Heinze Heise GmbH					
	Pedro Diniz et al., "Automatic Synthesis of Data Storage and Control S Engines", 2000, IEEE, pages 91-100	ructures for FPGA-based Computing					
	Markus Weinhardt et al., "Pipeline Vectorization for Reconfigurable Sy	· · · · · · · · · · · · · · · · · · ·					
	Lizy John et al., "A Dynamically Reconfigurable Interconnect for Array Processors", Vol. 6, No. 1, March 1998, IEEE, pages 150-157						
	Fineberg, Samuel et al., "Experimental Analysis of a Mixed-Mode Parallel Architecture Using Bitonic Sequence Sorting", Vol. 11. No. 3, March 1991, pages 239-251						
	Jacob, Jeffrey et al., "Memory Interfacing and Instruction Specification for Reconfigurable Processors", ACM 1999, pages 145-154						
	Ye, Z.A. et al., "A Compiler for a Processor With A Reconfigurable Fur ACM/SIGNA International Symposium on Field Programmable Gate App. 95-100.						
	Ling, X., "WASMII: An MPLD with Data-Driven Control on a Virtual Hardware," Journal of Supercomputing, Kluwer Acdemic Publishers, Dordrecht, Netherlands, 1995, pp.253-276.						
	Villasensor, J. et al., "Express Letters Video Communications Using Ra IEEE Transactions on Circuits and Systems for Video Technology, IEE 567.	pidly Reconfigurable Hardware," E, Inc. NY, December 1995, pp. 565-					
	Hedge, S.J., "3D WASP Devices for On-line Signal and Data Processin Wafer Scale Integration, pages 11-2)	g, 1994, International Conference on					
	Iseli, C., et al. "A C++ Compiler for FPGA Custom Execution Units Sy	·					
	Alippi, C., et al., "Determining the Optimum Extended Instruction Set Reconfigurable VLIW CPUs, IEEE., 2001, pp. 50-56						
	Dutt, Nikil et al., "If Software is King for Systems-on-Silicon, What's N 322-325						
	Piotrowski, Anton, "IEC/BUS, Die Funktionsweise des IEC-Bus und se Systemen", 1987, Franzis-Verlag GmbH, München, pp. 20-25						
•	Zhang, N. Et al., Architectural Evaluation of Flexible Digital Signal Pro Signals, Systems and Computers, 2000; Conference Record of the Thirt 29 October 2000 pp. 78-83.	y-Fourth Asilomar Conference, Bd.1					
	Fornaciari, W. Et al., System-level power evaluation metrics, 1997 Proc International Conference on Innovative Systems in Silicon, New York, 1	NY, October 1997, pp. 323-330.					
	Schmit, H. Ét al., Hidden Markov Modeling and Fuzzy Controllers in Fl Machined, 1995; Proceedings, IEEE Symposium on Napa Valley, CA, A	April 1995, pp. 214-221.					
	Simunio, T. Et al., Source Code Optimization and Profiling of Energy C Proceedings of the 13th International Symposium on System Synthesis,	onsumation in Embedded Systems, September 2000, pp. 193-198.					
XAMINER		DATE CONSIDERED					

INITIALS

AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.